More MOORE and MORE THAN MOORE MEETING FOR 3D

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INSTITUTE FOR ENERGY EFFICIENCY
Santa Barbara, California, December 2, 2011
CEA – LETI organization

French Nuclear Agency

15,000 Employees
3 billion € Budget

Technological Research

Fundamental Research

Electronuclear Energy Res.

Defense

3,200 Researchers

1,600 Researchers

Micro Nano Technology & integration in System

Software oriented system

New technology for Energy & Nanomaterials

* Grenoble

* Saclay

* Grenoble

S.Deleonibus  CEA-LETI December 2011
LETI: Mission and Focus

- A single mission:
  Create innovation
  & transfer it to industry

- A clear focus:
  - μ-nanotechnologies, with critical mass in Si
  - Advanced devices for new applications
in a few numbers - 2010

200 and 300mm Si capabilities
8,000 m² clean rooms
Continuous operation

1,600 researchers
1,000 permanent LETI staff

300 M€ budget
> 73% from contract
~ 40 M€ CapEx

350 new patents in 2010
Portfolio > 1,500 patents
32 start-ups
Since 2005: A complete set of research platforms...

CEA LETI (1600 CEA researchers) collaborating in MINATEC campus (>4000 researchers)

- MicroTechs for bio
- Design
- Education
- More Than Moore
- 200mm ‘CMOS’ new concepts & Beyond CMOS
- Nanoscale Characterization
- Incubation
- Advanced Research 100-200mm
- 300mm CMOS Integration & adv. modules

interacting daily with R & D platforms worldwide (ST Crolles, IBM Albany, …)
Budget: 1 Billion €
with investment: 150 M €

10,000 researchers
10,000 students

> 5,000 publications/year
> 500 patents/year
Outline

• Introduction: Trends and Hot Topics in Nanoelectronics
  • Nanoelectronics scaling and use of the 3rd dimension to continue Moore’s law.
  • Interfacing the Multiphysics World (More Than Moore) thanks to functional diversification
  • Building new systems and their packaging with a 3D tool box at a wafer level.
• Conclusions
Semiconductor Market applications successive waves

Quality of life, Social, Environment, Health, Energy, …associated to ICT

Source : Semico Research Corp. May 2004 IPI Report
Ecological Footprint of ICTs
reported by Intergovernmental Panel Climate Change (IPCC)

- Currently, 3% of the world-wide energy is consumed by the ICT infrastructure
  - which causes about 2% of the world-wide CO2 emissions
  - comparable to the world-wide CO2 emissions by airplanes or ¼ of the world-wide CO2 emissions by cars
- ICT: 10% of electrical energy in industrialized nations
  - 900 Bill. kWh / year = Central and South Americas
- The transmitted data volume increases approximately by a factor of 10 every 5 years

For ICTs, keep in mind:

\[ P = P_{\text{stat}} + P_{\text{dyn}} \]
\[ P_{\text{stat}} = V_{dd} \times I_{\text{off}} \quad \text{and} \quad P_{\text{dyn}} = CV_{dd}^2 f \]
Scaling: a success story...thanks to innovation

Moore’s law: 2X devices/year

Electronic Device Architectures for the Nano-CMOS Era
From Ultimate CMOS Scaling to Beyond CMOS Devices
Nomadic consumer and professional products: largest market share continuously increasing

Three major product families
(ITRS aware of CMOS scaling limits)

- High Performance (HP) \( t = C V / I \)
  - Connection to power network

- Low Operating Power (LOP)
  - Intermittent Nomadic Function

- Low Stand-by Power (LSTP) \( P_{\text{stat}} = V_{dd}xI_{\text{off}} \)
  - Permanent Nomadic Function

\[
P_{\text{dyn}} = C V_{dd}^2 f \\
P_{\text{tot}} = P_{\text{stat}} + P_{\text{dyn}}
\]
High growth with ‘More than Moore’ technologies: they require expertise in all technical domains and in-depth knowledge of the targeted markets.
EUV ($\lambda = 13.5$nm)

- 60% reflectivity for several hundreds of Si / Mo stacks with roughness precision < 3Å
- Placement of mirror and mask
- Photoresist

>100 M$  
100Wph  !!
System made of 13,000 electron beams working in parallel (MAPPER)

Key numbers 22nm node:

- HVM pre-alpha
- #beams and data channels: 13,000 / 110
- Spotsize: 25 nm / 35 nm
- Beam current: 13 nA / 0.3 nA
- Datarate/channel: 3.5 Gbs / 20 MHz
- Acceleration voltage: 5 kV / 5 kV
- Nominal dose: 30 μC/cm² / 30 μC/cm²
- Throughput @ nominal dose: 10 wph / 0.002 wph
- Pixel size @ nominal dose: 3.5 nm / 2.25 nm
- Wafer movement: Scanning / Static
System made of 13,000 electron beams working in parallel (MAPPER) (2)
Hot Topics in MOSFET technology

- Introduction of HiK and metal gate allows continued scaling and relaxes SiO2 gate leakage current related issues
  - $I_g$ added to SCE, DIBL, subthreshold leakage (LETI IEDM 2002, Intel IEDM 2005)
- Statistical dopant variability
  - number of dopants in the active area decreases with scaling
  - random distribution of channel dopants

Poisson’s law. Standard deviation:

$$\sigma_{doping} = \left( \frac{N}{Volume} \right)^{1/2}$$

Statistical fluctuations of threshold voltage: 150 mV decay for $V_T=200\text{mV}$ ($L_g=25\text{nm}$) !!

Major interest for Low Doped channels

S. Deleonibus et al. ESSDERC 1999
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32nm Low Power FDSOI Undoped channels

6T SRAM

300mm wafers

8 nm TSi
10 nm BOx

0.248\textmu m^2 SNM (1.2V)=140mV
0.179\textmu m^2 SNM (1.2V)=230mV

VDD=1V Ioff=6pA/\mu m

C.Fenouillet Beranger et al., IEDM 2007, VLSI Symp 2010
V.Barral et al., IEDM2007

Range = ±4 Å!

XUT+/- 5 Å - SOI thickness deviation

SOI Thickness
Max
Mean
Min

300mm wafers
Record-high $V_T$ matching performance

FDSOI Undoped channels vs. FinFET

Best trade-off between $V_T$ variations and gate length scaling compared to bulk MOSFETs and FinFETs

$\sigma_{\Delta V_t} = 34.5\text{mV}$
$\sigma_{V_t} = 24.5\text{mV}$
$A_{V_t} = 0.95\text{mV} \cdot \mu\text{m}$

$W = 60\text{nm}$
$L = 25\text{nm}$

$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}}$

O. Weber et al., IEDM 2008

(\( \sigma_{V_t} = \sigma_{\Delta V_t}/\sqrt{2} \) to compare measurements on pairs and on arrays of transistors in the literature)
Multi VT solutions for SOC design
UTBOX + Back bias ; Gate stack engineering

BOX = 10nm and VBB/ Ground Plane
N and PMOS: VT modulation of ≤200mV

VT tuning by gate stack engineering

F. Andrieu et al., VLSI 2010 Honolulu
O. Faynot et al., IEDM 2010 San Francisco, invited talk
Merits of FDSOI

Delay vs. Power x Delay
22% improvement/bulk (20nm)

Reachable Scaling rules
(TSi, TBOx)

O.Faynot et al, IEDM 2010, invited talk
L.Clavelier et al, IEDM 2010, invited talk
Thin Films Devices

Relaxing optimization scaling rule by architecture

- Bulk or thick SOI
- Planar
  - ThinSOI
  - Gate
  - Source
- Double-gate Planar or Finfet
- Trigate/nanowire

ThinSi = $\frac{1}{4} L_g$

ThinSOI

$T_{Si} = 2.5 \text{ nm}$

Barral et al. IEDM2007
Andrieu et al. VLSI2006

$T_{Si} = 1 \text{ to } 2 \ L_g$

Source

- $T_{Si} = \frac{1}{2} L_g$
- $T_{Si} = 1 \text{ to } 2 \ L_g$

Vinet et al. EDL 2005

Bernard et al. VLSI 2008
Dupré et al. IEDM 2008
Ernst et al. IEDM 2008

Jahan et al. VLSI2005

4.8 nm
3.4 nm
4.8 nm
3.4 nm

S.Deleonibus CEA-LETI December 2011
Stacked Multichannels and MultiNanowires « Top-Down » approach: device fabrication

- Si/Si$_{0.8}$Ge$_{0.2}$ superlattice epitaxy on SOI
- Anisotropic etching of these layers
- Isotropic etching of SiGe or Si
- Gate depositions HfO$_2$ (3nm), TiN (10nm), Poly-Si (200nm)
- Gate etching

S/D implantation
Spacer formation
Activation anneal
Salicidation

Standard Back-End of Line Processes

Top view of our device

Source
Nanowires
Drain
Gate

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Stacked Multichannels and MultiNanowires
« Top-Down » approach

- 3 multi-channels (MC)
- Tunable width
- Design flexibility to tune the conductance
- Stacked Multi-channels and Multi-Nanowires « Top-Down » approach

See for details:
T. Ernst et al, IEDM’06,’08 SSDM’07, ICIDT’08
E. Bernard et al. VLSI’08, ESSDER’07
C. Dupré et al, IEEE SOI Conference 07
Stacked Multichannels and MultiNanowires
« Top-Down » approach

Co-processed architectures with HfO₂, TiN Poly Si gate stack

(a) NWFET
(b) FET
(c) FinFET
(d) IG-FinFET

LETI top down approach for Low Power and High performance
- CV/I outperforms Planar in loaded environment
- Improved voltage gain (8GHz) wrt Planar
- Gate separation possible
- Transport properties in small nanowires

LETI: Dupré et al. IEDM 2008, San Francisco(CA)
Ernst et al., Invited talk IEDM 2008, San Francisco(CA)
Bernard et al, VLSI Symposium 2008 Honolulu
K.Tachi et al., IEDM 2010, San Francisco
Pervasion of Nanowire technology

Mass detection

Q=870 resonator
Gauge width = 80 nm

15 nm oscillator

Zeptogram mass resolution

$20\text{nm}$

Poly Si
SiO$_2$
Si$_3$N$_4$
SiO$_2$

$20\text{nm}$

$20\text{nm}$

3D NAND Flash Memories

Buffer solution at pH<7
Buffer solution at 7<pH<10
Buffer solution at pH>10

n-doped Si Metal Passivation Hole Electron

Chemical sensing

T. Ernst et al., IEDM 2008
Hubert et al., IEDM 2009
Tunnel FET Operation principle

N & P operation modes

- A single TFET device can operate either in n or p channel mode
  - N mode: \( V_{SD} > 0 \) & \( V_{GD} > 0 \)
  - P mode: \( V_{DS} < 0 \) & \( V_{GS} < 0 \)
SOI TFETs co-integrated with CMOSFETs

Experimental demonstration of Tunnel FET operations:

- **P mode**: $V_{DS} < 0$ & $V_{GS} < 0$
- **N mode**: $V_{SD} > 0$ & $V_{GD} > 0$

$L = 100\text{nm}; T = 300\text{K}$

F. Mayer et al., IEDM 2008, C. LeRoyer et al., ULIS 2009
TFET for Ultra Low Power outperforms CMOS
Offset/drain reduces Ioff (ambipolar current)

LETI: Mayer et al, IEDM 2008

Multigate improves Ion
EPFL: K. Boucart & A. M. Ionescu, ESSDERC 2006
Co-Integrating Heterogeneous orientation or materials

3D sequential process

- 4T SRAM
- Cold end process (bonding).
- Opportunities for other SC (Ge, III-V,...)
- Improved layout (40% area SRAM cell)
- Dynamically controlled VT:
  - Improved RNM and SNM

First heterogeneous orientation in 3D Si sequential integration
Enabled by use of wafer bonding by keeping low thermal budget

P. Batude et al., Best student Paper Award, IEDM 2009

P.Batude et al., Best student Paper Award, IEDM 2009
Sequential 3D: towards nanoscale devices

First demonstration of 3D sequential structure down to $L_G$ 50 nm

P. Batude et al, 2011 VLSI Tech Symp
P. Batude et al., IEDM 2011, Invited talk
Specific interest of low temperature process

The low temp. process (600°C) leads to a reduced EOT explained by a reduction of interfacial oxide growth

P. Batude et al, 2011 VLSI Tech Symp
Sequential 3D: Potential and Demonstrated Applications

High density logic applications

~ 1 node gain with same design rules for Front end levels

Heterogeneous integration

- Nanoelectronics & Photonics applications with Si-Ge Co-integration
- SRAM on top SOI logic, I/Os, analog on bottom bulk

3D memories

- SRAMs
- FLASH

P. Coudrain et al, IEDM 08,

P. Batude et al, VLSI09

P. Batude et al., IEDM 2009, Best Student Paper Award
3D-Xbar Memory stacked on Logic: towards NV Logic

Logic + Stacked NVM:  
High bandwith,  
Reduced Power consumption,…  
Reconfigurability  
ex: 32 nm node : > 1TB/s per 1mm²

Resistive switches  
Toshiba, Stanford Univ.: K.Abe et al, ICICDT 2008  
proven in 2D with Magnetic Tunnel Junctions,  
FeRAM Tohoku Univ., Hitachi:  
S.Matsunaga et al., Appl.Phys. Express(2008); ROHM
Advanced Devices and Systems
Future Vision

More than Moore

Diversified Logic
(association to Memory, Passives, Sensors, …)

3D stacked Mixed functions:
NV Logic + sensors/polymers
X bar

Memory storing (SRAM, NVM) –
ZDRAM

3D stacked devices

3D Nanowires

Low stress, HiD

Heat sink C

Beyond CMOS
(e-waves confinement, Spin electronics)

FDSOI
Std SOI
UTBOX
Nanowire

Dual channel xsSOI(N)/ Ge(P)

FDSOI

Logic

More Moore

HP options

22nm

16nm

11nm

< 11nm


Carbon electronics (CNT, Graphene, Diamond)

Transfer to Industry Development

S.-P. Deleonibus CEA-LETI December 2011
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### Opportunities for other materials on Silicon

**Electronic Device Architectures for the Nano-CMOS Era**
From Ultimate CMOS Scaling to Beyond CMOS Devices
Editor: S. Deleonibus, Pan Stanford Publishing, July 2008

<table>
<thead>
<tr>
<th>Material</th>
<th>$\mu_n$ (cm$^2$/V·s)</th>
<th>$\mu_p$ (cm$^2$/V·s)</th>
<th>$s_{th}$ (W/m·K)</th>
<th>Rel. K</th>
<th>Eg(eV)</th>
<th>$v_{sat}$ (10$^7$ cm/s)</th>
<th>$n_i$ (cm$^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1400</td>
<td>500</td>
<td>141</td>
<td>11.9</td>
<td>1.12</td>
<td>0.86</td>
<td>$2 \times 10^{10}$</td>
</tr>
<tr>
<td>Silicon compatible</td>
<td>Well established high (&gt;40 yrs experience) Oxidizable !</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ge</td>
<td>3900</td>
<td>1900</td>
<td>59.9</td>
<td>16</td>
<td>0.66</td>
<td>0.60</td>
<td>$2 \times 10^{13}$</td>
</tr>
<tr>
<td>Silicon compatible</td>
<td>Available in all fabs GaAs lattice constant matching</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GaAs</td>
<td>8500</td>
<td>400</td>
<td>55</td>
<td>12.9</td>
<td>1.42</td>
<td>0.72</td>
<td>$2.1 \times 10^6$</td>
</tr>
<tr>
<td>InGa$<em>{0.47}$As$</em>{0.53}$</td>
<td>12 000</td>
<td>300</td>
<td>5</td>
<td>13.9</td>
<td>0.74</td>
<td>0.6</td>
<td>$6 \times 10^{11}$</td>
</tr>
<tr>
<td>InSb</td>
<td>77000</td>
<td>850</td>
<td>1.8</td>
<td>16.9</td>
<td>0.17</td>
<td>5</td>
<td>$2 \times 10^{16}$</td>
</tr>
<tr>
<td>C-Diamond sp3</td>
<td>2200</td>
<td>1800</td>
<td>2000</td>
<td>5.7</td>
<td>5.47</td>
<td>2.7</td>
<td>$1 \times 10^{12}$</td>
</tr>
<tr>
<td>Graphene (CNT) sp2</td>
<td>$10^4$-$10^5$</td>
<td>$10^4$-$10^5$</td>
<td>1000</td>
<td>5.7</td>
<td>Semi-metal</td>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

Highest $\mu_n$ but Worst $\mu_n/\mu_p$!!

Highest $\sigma_{th}$

Most compact logic, Interconnect

Passive layer combine w BOX (thermal shunt)

BTBT

TFET/νW
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• Conclusions
### NEMS scaling laws. Is it worth scaling?

- resolution increases
- sensitivity decreases (SBR,SNR) => arrays, actuation,…
- figures of merit pressure and vacuum quality dependent

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Scaling rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>mass</td>
<td>$k^3$</td>
</tr>
<tr>
<td>stiffness</td>
<td>$k$</td>
</tr>
<tr>
<td>resonant frequency</td>
<td>$k^{-1}$</td>
</tr>
<tr>
<td>mass responsivity</td>
<td>$k^{-4}$</td>
</tr>
<tr>
<td>energy consumption</td>
<td>$k^3$ [rough estimate]</td>
</tr>
</tbody>
</table>

\[
\delta m = \frac{M_{\text{eff}}}{Q} \cdot 10^{-(DR/20)}
\]

\[
DR \propto \sqrt{\sum \frac{S_{\text{noise}}}{P_{\text{act}}} = \frac{1}{\text{SNR}}}
\]

ML Roukes et. al. APL (2005)

\[
M_{\text{eff}} \propto l \cdot w \cdot t
\]

\[
K_{\text{eff}} \propto \frac{t^3}{l^3}
\]

\[
f_0 \propto \sqrt{\frac{K_{\text{eff}}}{M_{\text{eff}}}} \propto \frac{t}{l^2}
\]

\[
\mathcal{R} = \frac{\partial f_0}{\partial M_{\text{eff}}} = -\frac{f_0}{2M_{\text{eff}}}
\]

\[
E_P \approx \frac{1}{2} K_{\text{eff}} \cdot x_{\text{Max}}^2
\]

and \( x_{\text{Max}} \propto t \)
Nanowire used for mass detection

- First 200 mm wafers with 3.5 millions NEMS
- Association Nanowire/Resonator ; Cantilever arrays

CMOS compatible

LETI: T.Ernst et al., IEDM 2008, Invited talk
L. Duraffourg et. al, APL 92, 174106 (2008)
M&NEMS co-integrated devices platform for 3D sensing

3-axis accelerometer
\[ \Delta R/R < 5 \times 10^{-4} \ (\pm 1 g) \]
Linearity < 0.3\% (0 and 200MPa)
S < 1 mm\(^2\) (3 axis)

3-axis gyroscope
\[ F_0 \approx 20.3 \text{ kHz} \]
Q > 100,000 S = 0.8 mm\(^2\) / axis

3D magnetometer
- Resol 20-80 nT/√Hz
- Lin 4.5 mT
- S = 0.25 mm\(^2\)/axis

Microphone

Pressure sensor

Area ÷ 4 vs SoA

Nanobeams

P. Robert et al, 2009 IEEE Sensors
D. Ettelt et al, 2011 Transducers
NEMS switch

"high" speed


“high” speed

high on/off

from D. Tsamados et al. Solid-State Elec. 52 1374 (2008)

low power

 bistable memory

from Q. Li et al., IEEE Nano 6(2) 256-262 (2007)

“high” speed rf


high on/off low power logic

from D. Tsamados et al. Solid-State Elec. 52 1374 (2008)

from Q. Li et al., IEEE Nano 6(2) 256-262 (2007)
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System On Wafer: Heterogeneous co-Integrated Systems

(Parallel 3D)

Commercial products
- image on board VGA camera,
- mixed nodes & modes,
- high density TSV

Cross talks:
- delay, matching,
- power dissipation
  (global temp. increase, hot spots, reliability, …)

Multiphysics

New Progress Laws
- application specific

Energy source converter
Wafer level packaged MEMS
MEMS

80 µm diameter TSV imagers packaging

Via belt technology
MEMS + IC stack
Ultra flat 3D
Chip stacking(TSV)

On Silicon
Active Silicon interposer
account wafer level

Commercial products
- image on board VGA camera,
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Cross talks:
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  (global temp. increase, hot spots, reliability, …)

Multiphysics

New Progress Laws
- application specific
3D Integration: from imagers to advanced 3D ICs

Mixed Signal
Digital/Analog

ST - LETI collaboration

Die to substrate copper pillars

Die to Die Copper pillars

Thinned wafer (~100 µm)

Diam 60µm
Thick 120 µm

Via Last TSV (Aspect Ratio 2:3)

Active Silicon interposer

3D high density

VGA cameras (300k pixels)

2001

2008

ST - LETI collaboration

3D-IC

Memory, Processors, Imagers with high density TSV, NEMS...

Image-on-Board
Photonics Integration on Silicon. The building blocks.

- Optical modulator
- Photodetector
- MUX & DEMUX
- Waveguide
- Grating coupler
- In-plane coupler
- Laser source
- Optical switch

LETI: L. Fulbert ESSDERC 2011, Invited talk
## Application Drivers

<table>
<thead>
<tr>
<th>Application</th>
<th>Form Factor</th>
<th>Cost</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MOBILE WIRELESS</strong></td>
<td>Ultra small TV Tuner, Sharp</td>
<td>Full tranceiver on Chip, Antenna+RF+ Baseband, Leti</td>
<td>Nokia N82, 5Mpixel Video capture, coding, transmission</td>
</tr>
<tr>
<td><strong>CONSUMER</strong></td>
<td>Computer control using thoughts</td>
<td>128 GB SSD, Toshiba</td>
<td>One Chip SetTopBox (STM)</td>
</tr>
<tr>
<td><strong>HEALTH</strong></td>
<td>Quad Core Intel</td>
<td></td>
<td>Intel's Teraflop Chip</td>
</tr>
<tr>
<td><strong>COMPUTING &amp; STORAGE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>AUTOMOTIVE</strong></td>
<td></td>
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</tr>
</tbody>
</table>

Great focus on packaging & integration
Conclusion: Nanoelectronics CMOS from Devices to Systems Perspectives

- **Si CMOS**: Nanoelectronics Base platform beyond ITRS
- **Durable Low Power solutions**: health, environment, quality of life, energy, IST,…
- **Low Power consumption**: major challenge (sub 1V VDD CMOS).
  
  => Device/system architecture optimization:
  
  Thin Films Gate All Around nanowires, low slopes, layout, 3D

  => Opportunities for new materials on Silicon
  
  (Ge, revised low BG III-V, Carbon,…) to co-integrate from LSTP to HP.

- **Heterogeneous 3D co-Integration on Si, Low Power**: Monolithic/Sequential 3rd dimension in device. New active materials Reconfigurability with NVM; NV Logic
  
  System On Wafer: 2 to 3D heterogeneity functions & chips
Thank you for your attention
Merci de votre attention
Electronic Device Architectures for the Nano-CMOS Era
From Ultimate CMOS Scaling to Beyond CMOS Devices
edited by Simon Deleonibus (CEA-LETI, France)
Cloth July 2008 978-981-4241-28-1

★ Discusses the scaling limits of CMOS, the leverage brought by
new materials, processes and device architectures (HiK and
metal gate, SOI, GeOI, Multigate transistors, and others), the
fundamental physical limits of switching based on electronic
devices and new applications based on few electrons operation

★ Weighs the limits of copper interconnects against the
challenges of implementation of optical interconnects

★ Reviews different memory architecture opportunities through
the strong low-power requirement of mobile nomadic systems,
due to the increasing role of these devices in future circuits

★ Discusses new paths added to CMOS architectures based on
single-electron transistors, molecular devices, carbon nanotubes,
and spin electronic FETs

Available at Amazon.com or
any good bookstores.