Miniaturized Power Conversion Circuits for New Frontiers in IoT and Beyond

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What is a Power Converter?

- A circuit that changes the level of the input voltage ($P_{\text{out}} \sim P_{\text{in}}$) and converts electric power from one form to another.

![Diagram showing a DC/DC converter and a DC/AC converter with voltage levels and solar panel.

- $V_{\text{BAT}} \sim 4\text{V}$
- $V_{\text{DD}} \sim 1\text{V}$
- Energy Harvester
- DC/DC
- Solar panel
- $0.4\text{V}$
- $1\text{V}$
- $60\text{Hz}$
Why Innovations are Needed in Power Converters?

- **Power consumption**
  - Power converters often constitute a major factor determining the system efficiency

  
  - In an LED light bulb, 10-30% of the input power doesn’t reach the LED array and rather gets dissipated as heat in the power conversion

- **Size & Cost**
  - Power converters typically occupy a large fraction of the overall system

*The subtle circuitry behind LED lighting, IEEE Spectrum*
Why Innovations are Needed in Power Converters?

- In solar systems, the cost of the power converters is typically higher than the PV module itself.

200W Solar Panel Kit

Hardware cost breakdown of a residential PV system

[*National Renewable Energy Laboratory 2017]
Why Innovations are Needed in Power Converters?

- Roadway-powered electric vehicles

Electric vehicles will be able to travel reliably over thousands of miles (~10hrs are needed to recharge a Tesla car)

Enormous cost to build a freeway with thousands of miles of coils
DC-DC converters (power management circuits) are a major factor determining the system size & power

- DC-DC converters are ~40% of electronic board
- Consume ~ 22% of energy
Making power converters smaller & less expensive

- **Use capacitors instead of inductors to perform power conversion**

A capacitor can carry the same amount of energy in ~ 150× smaller size†

[†Yutian Lei, TPEL’18]

Capacitors can realize a power converter in orders-of-magnitude smaller size & 10x lower cost
Problem of Prior SC Solutions

- Prior solutions succeeded in employing capacitors instead of inductors to make power conversion smaller
  - however, they are not as efficient as the inductor-based converters
Research Interests

- Goal: to make power conversion efficient, smaller, and cheaper

### Research interests by the employed scheme

**High efficiency & low cost power conversion using new switched capacitor circuit topologies developed by:**
- reproducing efficient mathematical formulas in a switched network form
- digital signal processing of the power flow

**Power conversion using new materials**
- New high-voltage fast GaN switches (Umesh Mishra)
- New passives (Kaustav Banerjee)

### Research interests by application

- LED drivers
- Solar & renewable power electronics
- Power management ICs
- mmWave envelope tracking
- picoWatt power electronics for biomedical applications
Outline

- Power conversion based on new switched capacitor circuit topologies

  - Miniaturizing **DC-to-DC** conversion:
    - Recursive Binary Switched Capacitor DC-DC Converters

  - Miniaturizing **DC-to-AC** conversion:
    - Switched Capacitor Adiabatic Clocking
Inductor- vs. Capacitor-Based DC-DC Converters

- Why SC is not as efficient?
  - SC converters suffer from a fixed $V_{in}$-to-$V_{out}$ conversion gain

**L-based DC-DC converter**

$V_{in} \times \text{Duty} \rightarrow V_{out}$

*has a variable gain* = duty

**C-based DC-DC converter**

$V_{in} \times 2 \rightarrow V_{out}$

*has a fixed gain* = 2
Why a Variable $V_{in}$-to-$V_{out}$ Gain is Required?

- $V_{BAT}$ decays with operating time
- SC fixed gain, e.g. 1/2
- SC cannot maintain $V_{out}$ at desired level (2V) as $V_{BAT} \downarrow$ due to its fixed gain
- $L$-based Converter increases its gain as $V_{BAT} \downarrow$ to keep $V_{out} = 2V$
Why SL has a Variable Gain?

Use an LC filter to extract the DC component in a rectangle voltage

Gain can be changed by changing duty cycle $D$
SC converts voltage by connecting charged capacitors in parallel & series

C is connected in parallel to $V_{in}$

Volt. across C charges to $V_{in}$
Why SC Suffers From a Fixed Gain?

Connect C in series with $V_{in}$

$V_{out} = 2 \times V_{in}$

$V_{in}$

previous connection

$SC$ has a fixed gain ($V_{out}/V_{in} = 2$)
Prior Solution 1: SC Output Resistance Regulation

- How to mitigate the SC fixed gain? → Add a variable $R_{out}$ in series with the SC

\[
\begin{align*}
V_{in} & \rightarrow \frac{V_{in}}{2} \\
\div 2 & \text{ SC} \\
& \rightarrow 0 \\
R_{out} & \rightarrow \text{large} \\
& \rightarrow \text{0} \\
\text{Load} & \\
V_{out} & \rightarrow V_{in}
\end{align*}
\]
Prior Solution 1: SC Output Resistance Regulation

\[
\frac{1}{2} \text{SC} \quad \text{R}_{\text{out}} \quad V_{\text{out}} \quad + \Delta V
\]

- **R_{out}** introduces required **V_{out}** by burning \(\Delta V\) into heat.
- **SC \(\eta\)** is max, when \(R_{out} \sim 0\).
- **SC \(\eta\)** ↓ as \(R_{out} \uparrow\) (\(V_{out} \downarrow\)) due to increased loss.
Prior Solution 1: SC Output Resistance Regulation

SC efficiency is high across a narrow $V_{out}$ range.

Inductive DC-DC $\eta$

SC is not as efficient as the SL.
Instead of using a single SC network
Prior Solution 2: Use Multiple Gains

Features:
- Use multiple SC networks
  → multiple gains
  → more flat $\eta$ as SL

Enable the SC that provides the highest $\eta$

Options:
- SC Network for 1/3
- SC Network for 1/2
- SC Network for 2/3
Prior Solution 2: Use Multiple Gains

Problem: efficiency drops > 20% in-between 3 gains as compared to inductive converter

Inductive DC-DC
Solution 3: Employ more SC networks to provide gains between the 3 gains to fill $\eta$ gaps (present R&D)

\[ \Delta V_{\text{out}} \equiv \text{resolution} \]

N-bit resolution
\[ \Delta V_{\text{out}} = \frac{V_{\text{in}}}{2^N} \]
Solution 3: Use Many Gains

Efficiency of higher-resolution gains falls below the efficiency of lower-resolution gains

$\eta$ of 3-bit gains doesn’t fill gaps

- 4-bit
- 5-bit
Capacitive DC-DC converter couldn’t replace the L-based converter as the industry standard.
Advantage of topology: efficiency of higher resolution gains doesn’t fall below lower resolution gains.
**Proposed Recursive SC Topology**

- Idea: to achieve fine-resolution gains, connect multiple divide-by-2 SC converters either in cascade or stack†

\[ \frac{1}{2} \div 2 \div 2 \div 2 \div 2 \div 2 \div 2 \div 2 \]

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[†Loai Salem et al., IEEE Journal of Solid-State Circuits’14, special issue]

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RSC 2-bit

Cell in Stack

RSC 3-bit

Cell in Cascade
Proposed Recursive SC Topology

- Connect multiple divide-by-2 SC converters either in cascade or stack†

\[
\frac{V_{in}}{2} = \frac{V_{in}}{4}
\]

[†Loai Salem et al., IEEE Journal of Solid-State Circuits’14, special issue]
Proposed Recursive SC Topology

- Connect multiple divide-by-2 SC converters either in cascade or stack†

\[ \Delta V \text{ across } 2^{nd} \text{ stage} \]

\[ \frac{V_{in}}{2} \]

\[ \text{V}_{\text{in}} \]

\[ \text{V}_{\text{out}} = \frac{V_{in}}{2} + \frac{V_{in}}{4} = \frac{3V_{in}}{4} \]

2\text{nd stage is stacked on 1\text{st} stage}

2\text{nd stage divides } \Delta V \text{ by 2}

[†Loai Salem et al., IEEE Journal of Solid-State Circuits’14, special issue]
Proposed Recursive SC Topology

- By cascading & stacking more SC stages, finer conversion resolutions can be achieved
In the new topology, the efficiency of higher resolution gains doesn’t fall below lower resolution gains.
In prior SC topologies, the power loss ↑ as the gain resolution ↑. In Recursive SC, the power loss converges to an upper bound.

Normalized $P_{\text{loss}}/\Delta V$ diverges as $\Delta V_{\text{out}}/2$ increases with resolution ↑.

[Loai Salem et al., Journal of Solid-State Circuits’14]
Why does the loss converge in this topology?

Two cascaded linear regulators

\[ P_{\text{loss}} = I_{\text{out}}^2R + I_{\text{out}}^2R \]

Two cascaded divide-by-2 SC

\[ P_{\text{loss}} = \frac{I_{\text{out}}^2R}{4} + I_{\text{out}}^2R \]

2\textsuperscript{nd} SC stage loads only half of \( I_{\text{out}} \) on 1\textsuperscript{st} stage instead of the total \( I_{\text{out}} \)
Why does the loss converge in this topology?

**A general N cascade in the Recursive topology**

Each stage loads only half of it $I_{out}$ on its previous neighbor
Why does the loss converge in this topology?

Stage Power Loss

\[ P_N = i_N \Delta V_N \quad \ldots \quad P_4 = i_4 \Delta V_4 \]

\[ P_3 = i_3 \Delta V_3 \]

\[ P_2 = i_2 \Delta V_2 \]

\[ P_1 = i_1 \Delta V_1 \]
Why does the loss converge in this topology?

In conventional cascade, each stage current is the same.

Total $P_{\text{loss}} = P_1 + P_2 + \ldots + P_N = \text{summation of a decreasing loss}$

$P_N = I_{\text{out}}/2^{N-1} \times \Delta V$

$P_1 = I_{\text{out}} \times \Delta V$

$P_2 = I_{\text{out}}/2 \times \Delta V$

$P_3 = I_{\text{out}}/4 \times \Delta V$

$P_4 = I_{\text{out}}/8 \times \Delta V$
Why large cascade of stages doesn’t increase loss in RSC

In conventional cascade, each stage current is the same

In conventional cascade, $P_{\text{loss}}$ diverges

In Recursive, total $P_{\text{loss}}$ converges to an upper bound with large cascading for high resolution gains ($N$)

$\sum P_k$

$I$ & $P_{\text{loss}}$ of each stage in Recursive

$P_N = i_N \times \Delta V$

$P_1 = i_1 \times \Delta V$

$P_2 = i_2 \times \Delta V$

$P_3 = i_3 \times \Delta V$

$P_4 = i_4 \times \Delta V$
Proposed Topology Advantage

Recursive topology can fill the efficiency gaps while others cannot

Enables a capacitive replacement for SL

6-bit Recursive

Inductive DC-DC

Other topologies

Efficiency [%]

V_{out}
Recursive SC Proof-of-Concept Prototype

**fabricated microchip**

<table>
<thead>
<tr>
<th>Chip Summary</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>process</td>
<td>CMOS 0.25µm</td>
</tr>
<tr>
<td>resolution</td>
<td>15 gains, 4-bit</td>
</tr>
</tbody>
</table>
Measured Efficiency from the Fabricated Microchip

- Prototype was measured from $V_{in}=2.5V$ while supplying $I_{out}=2mA$

Recursive SC provides semi-flat efficiency, like the inductive converter
Outline

- *Power conversion based on new switched capacitor circuit topologies*

  - Miniaturizing **DC-DC** conversion:
    - Recursive Binary Switched Capacitor DC-DC converters

  - Miniaturizing **DC-AC** conversion:
    - Switched Capacitor Adiabatic clocking
Problem: Global Clock Distribution $P_{\text{Loss}}$

- Clock distribution in high-end µProcessors consumes a large fraction of the total chip power.

CLK-tree & grid span the entire µChip, e.g. 10 mm.

Their wires’ capacitance adds up & becomes very large.
Problem: Global Clock Distribution $P_{Loss}$

- Such large $C_{CLK}$ is charged/discharged every CLK cycle using buffers.

Large Charging/discharging loss results

$$P_{CLK} = C_{CLK} V_{DD}^2 f_{CLK}$$

This is why such $P_{CLK}$ constitutes a large percentage ($\sim 20\%^{\dagger}$) of the Chip power consumption.

Such $P_{CLK}$ cannot be reduced through CLK gating since loss is in the distribution itself.

$[^{\dagger}]$Sathe, JSSC 2013
Prior Solution: Resonant Clocking

- Resonant Clocking: add an inductor $L$ in parallel to $C_{CLK}$ to cancel its reactance $(1/\omega_0 C_{CLK})$ at $f_0$.

[Chan, ISSCC 2004]
Resonant Clocking Problems

- $P_{CLK}$ reduction is across a limited $f_{CLK}$ range around $f_o$
- Requires inductor(s) which occupies large area on chip

**Graph:**
- **Static CMOS:**
  - $C_{CLK} V_{DD}^2 f_{CLK}$
- **Resonant frequency ($f_o$)**
- **Limited frequency range with reduced $P_{CLK}$**
Proposed Solution

How to reduce CLK power without *inductors*?

\[ P_{CLK} = C_{CLK} V_{DD}^2 f_{CLK} \]
Proposed Solution: Adiabatic Charging

- Adiabatically charge/discharge $C_{CLK}$ through a staircase voltage to reduce clock power

$P_{CLK} = C_{CLK} V_{DD}^2 f_{CLK}$

$P_{CLK} = \frac{C_{CLK} V_{DD}^2 f_{CLK}}{3}$

[†Loai Salem et al., ISSCC’17]
Proposed Solution: Adiabatic Charging

- Adiabatically charge/discharge \( C_{CLK} \) through a staircase voltage

\[
P_{CLK} = C_{CLK} V_{DD}^2 f_{CLK}
\]

\[
P_{CLK} = \frac{C_{CLK} V_{DD}^2 f_{CLK}}{N}
\]

Number of CLK-waveform steps

[†Loai Salem et al., ISSCC'17]
Proposed Solution: Adiabatic Charging

Adiabatic Clocking enables flat power savings across the entire frequency range without an inductor
Resonant vs. Adiabatic CLK Waveforms

- Adiabatic clocking can provide sharp rise/fall times

![Diagram showing comparison between resonant and adiabatic waveforms. The adiabatic waveform has a sharper rise and fall time compared to the resonant waveform. The diagram indicates a 50% T_CLK rise/fall time.]
How to Synthesize a Staircase Voltage?

Initial idea to synthesize the staircase:

- 4 switches
- 2 voltages sources at $V_{DD}/3$ and $2V_{DD}/3$
How to Synthesize a Staircase Voltage?

- The switches s1, s2, s3, s4 are sequentially turned on to charge $C_{CLK}$ to $V_{DD}$
How to Synthesize a Staircase Voltage?

- Turn off s2 and turn on s3 to charge $C_{CLK}$ to $2V_{DD}/3$
How to Synthesize a Staircase Voltage?

- Turn off s3 and turn on s4 to charge $C_{CLK} \rightarrow V_{DD}$
How to Synthesize a Staircase Voltage?

- Switch s4, s3, s2, s1 in the reverse order to discharge $C_{CLK}$:

MAIN PROBLEM: this requires 2 external supplies!
Replace the voltage sources with capacitors

How would C1 & C2 provide $V_{DD}/3$ & $2V_{DD}/3$?
Charge-Flow-Based Analysis
The 4-phase Switched Capacitor KVL Solution

- **Kirchhoff's Voltage Law Analysis:**
  these 4 phases result in 4 KVL equations:

\[
\begin{bmatrix}
-C1-C_{CLK} & C1 & 0 & 0 \\
C1 & -C1-C_{CLK} & 0 & C_{CLK} \\
C_{CLK} & 0 & -C2-C_{CLK} & C2 \\
0 & 0 & C2 & -C2-C_{CLK} \\
\end{bmatrix}

\begin{bmatrix}
V_{C1_UP} \\
V_{C1_DN} \\
V_{C2_UP} \\
V_{C2_DN} \\
\end{bmatrix}

= \begin{bmatrix}
0 \\
0 \\
0 \\
-C_{CLK}V_{DD} \\
\end{bmatrix}
\]

- **KVL solution** is \( V_{C1} = V_{DD}/3 \) & \( V_{C2} = 2V_{DD}/3 \)
- **No need for external supplies!**
Initially $V_{C1}=V_{C2}=0$

$V_{C1}$ & $V_{C2}$ naturally settle at $V_{C1}=V_{DD}/3$ & $V_{C2}=2V_{DD}/3$

Start up

$f_{CLK} = 1\text{GHz}$
Losses Due to Capacitors’ Voltage Ripple

Charge-sharing between $C_{CLK}$ & C1 or C2 results in a voltage ripple across C1 or C2

When $C_{CLK}$ is charged through C2

$V_{initial} = \frac{2V_{DD}}{3}$

$\Delta V$

$V_{final}$

$V_{initial} = \frac{V_{DD}}{3}$

$C_{CLK}$
Losses Due to Capacitors’ Voltage Ripple

- The voltage ripple across C1 & C2 results in extra losses:
  - Adiabatic CLK loss is not only $C_{CLK} V_{DD}^2 f_{CLK}/3$
  - But also, ripple loss across C1 & C2

\[ E_{CLK\_Adiabatic} \approx \frac{1}{3} E_{StaticCMOS} + C_1 \Delta V_1^2 + C_2 \Delta V_2^2 \]

How to reduce?
Capacitors’ Voltage Ripple Loss Reduction

Answer: increase the capacitance of C1 and C2

\[ E_{\text{adiabatic}} \approx \frac{1}{3} E_{\text{staticCMOS}} + C_1 \Delta V_1^2 + C_2 \Delta V_2^2 \]

How much the required \( C_1 + C_2 \)?
Optimal $C_{total} = C1 + C2 \sim 7 \times C_{CLK}$
The resonant clocking not only requires inductor(s) but also larger capacitance $C_D > 10 \times C_{CLK}$ and $C1 + C2 < 7 \times C_{CLK}$.
The 4 switches can be implemented using 2 CMOS inverters.
## Adiabatic Clock Prototype

A prototype microchip was fabricated

<table>
<thead>
<tr>
<th>Technology</th>
<th>45nm SOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load</td>
<td>Pipelined array of 64b MACs (15pF)</td>
</tr>
</tbody>
</table>

**Load**

- 32x 64b MACs
- Resonant CLK driver area ~ 100% of $A_{LOAD}$
- SC CLK driver area < 6.2% of $A_{LOAD}$ (no inductors)

16x drivers + HoC

100pF

138x129μm

38x24μm

550μm
Flat power savings > 42% across the entire 10M-2GHz: almost half of the CLK power is saved.
Measured Clock Power Savings

- At $V_{DD} = 0.4$ V (near threshold operation)

Successful operation near-$V_{th}$ with > 34.4% savings, while resonant typically fails due to $R_{on}$
Prior resonant clocking schemes versus $f_{CLK}$ & $V_{DD}$ dynamic ranges

All resonant clocking schemes are limited below $20 \times f_{CLK}$ & $1.8 \times V_{DD}$ ranges
Resonant vs. Proposed Adiabatic Clocking

2000× dynamic $f_{CLK}$ range
- near $v_{th}$ to full $V_{DD}$ operation

All resonant clocking schemes are limited below 20× $f_{CLK}$ & 1.8× $V_{DD}$ ranges

- 2000× dynamic $V_{DD}$
- $f_{CLK}$ range

$V_{DD}$: 2.5×
$P_{save}$ = 55.6% This Work

$< V_{DD}$: 1.8×

$< f_{CLK}$: 20×
$P_{save}$ = 47% Rahman, ISSCC 16

- 33% Restle, ISSCC 2014

- 30% Sathe, ISSCC 2012

- 25% Chan, ISSCC 2008
Approach: develop new SC circuits that reproduce efficient mathematical formulas to make power conversion less expensive but without losing the inductive converter’s efficiency

<table>
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<tr>
<th>Circuit Topology</th>
<th>Scheme</th>
<th>Added Value</th>
</tr>
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<tbody>
<tr>
<td><strong>Recursive Binary SC dc-to-dc converter</strong></td>
<td>Make each stage current follow a subsiding binary series</td>
<td><em>First SC topology of semi-flat efficiency as the inductor-based converter</em></td>
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<tr>
<td><strong>Adiabatic Clocking</strong></td>
<td>Make capacitors voltages at equal steps by shaping the KVL system using a multi-state network</td>
<td>Flat clock power reduction without using a single inductor</td>
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