Compliant III-V on (001) Si substrates for direct laser growth

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III-V on Si: Toward a heterogeneous world

- **Opportunities**
  - III-V logic with advanced CMOS
  - Hybrid integrated circuits with on-chip interconnect

- **Challenges**
  - Material: III-V on Si
  - Device: III-V logic device technology and integrated light sources

*Nature Materials 6, 810 - 812 (2007)*

*IEDM 2013, p.699*
III-V/Silicon Photonic On-Chip WDM Network

Epitaxially grown Quantum Dot laser and Epitaxially grown III-V-on-Si photodetector

Source: Andrew Poon, HKUST
Silicon as growth substrates for III-V Devices

- Low cost manufacturing: high quality Si wafers up to 12-inch (300mm) commercially available
- Silicon technologies are the most advanced and cost effective
- Integration of high performance III-V devices with Si logics and memory circuits, Si photonics, lighting drivers……
- No need for brittle and expensive InP substrates
Microdisk lasers on silicon

* III-V on silicon
+ Quantum Dots
+ Whispering Gallery Mode (WGM) Resonant cavity

- High quality factor
- Small footprint
- Low threshold /power
- In-plane/waveguide coupling
What are the choices?

- **Wafer Bonding**
  - Sample size difference
  - Alignment
  - Yield
  - Volume manufacturing

- **Direct growth**
  - Material issues
  - Process integration
Challenges: Heteroepitaxy of III-V on Si

- High-density defects
  - 4-8% lattice mismatch (dislocations & stress)
  - Thermal expansion coefficient mismatch (stress)
  - Polar on non-polar (APD)
- Buffer thickness: cost, process throughput
- Poor thermal conductivity of ternary alloy buffer

Source: IEEE spectrum
Review: Defect Engineering Approaches

Nucleation
Two-step growth

Compositional graded buffer
* J. Crys. Growth 324, 103 (2011)

Interlayer/superlattices
* Appl. Phys. Lett. 73, 2917 (1998)

LT nucleation growth

Si

HT-epi-layer growth

Si

➢ Combined with thermal annealing


FIG. 2. Mechanisms of dislocation motion in GaAs/Si.
Blanket epitaxy: InP/GaAs/Si

- Direct growth of InP on planar Si: high defect density
- Ge, superlattices, graded compositions commonly used
- Our approach: GaAs as intermediate buffer between Si and InP
MOCVD Systems @ HKUST for III-As/P/Sb Alloy growth

AIX200/4 Reactor on single 4 in substrate

CCS 6x2" or single 4” /6”
As/P based materials
Blanket epitaxy @ HKUST: InP/GaAs/Si

- **Two-step growth method**
  - Surface/Kinetic limited regime at *low temperature* (LT)
    - Full coverage/better stress release
  - Mass transport limited regime at *high temperature* (HT)
    - Improved crystalline quality

Diagram showing the growth process with layers labeled:
- HT-InP buffer
- InGaAs
- HT-GaAs buffer
- LT-InP
- LT-GaAs
- Exact Si (001) substrate

Graph showing temperature change over growth time:
- LT-GaAs
- LT-InP
- HT-GaAs
- HT-InP
**High-electron mobility transistors**

<table>
<thead>
<tr>
<th>Inverted HEMT (iHEMT)</th>
<th>Conventional HEMT</th>
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<tbody>
<tr>
<td>( \text{In}<em>{0.52}\text{Al}</em>{0.48}\text{As} )</td>
<td>( \text{In}<em>{0.52}\text{Al}</em>{0.48}\text{As} )</td>
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<tr>
<td>( \text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As} ) channel</td>
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<td>InP/GaAs/Si compliant substrate</td>
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Our planar buffer since 2008

Delta-doping

500 nm

Defect Trapping in Nano-patterns

- Trapping most of the threading dislocations
GaAs-on-V-grooved (001) Si

- Start with exact (001) Si substrate
- V-grooved Si (111) surfaces

- Antiphase-domain-free, low density defect, smooth morphology...

*Q. Li et al., Appl. Phys. Letts. 106 (7), 072105, 2015*
Cross-sectional TEM comparison with offcut Si

Dislocation lines punching through the active region will create non-radiative recombination centers

GaAs on V-groove patterned on-axis (001) Si

GaAs on planar offcut (001) Si

- Defects generated at the GaAs/Si hetero-interface were trapped by the V-grooved structure on GoVS template
- A larger amount of stacking faults (SFs) and threading dislocations were observed in the GaAs buffer in the offcut Si template.
Cross-sectional TEM comparison

- GaAs on V-groove patterned on-axis (001) Si

- GaAs on planar offcut (001) Si
Typical plan-view TEM comparison

The TDD was determined by counting numbers of dislocations in a given area based on an average number of 30 plane-view TEM images for accuracy.

- A three-fold reduction of threading dislocation using V-grooved Si
- V-grooved Si: $2.8 \times 10^8$/cm$^2$
- Offcut Si: $8.3 \times 10^8$/cm$^2$
Growth template: GaAs-on-V-grooved Si (GoVS)

- V-grooved nano-patterned (001) Si substrate
  - No Ge. No offcut.
  - Aspect ratio trapping combined with epitaxial lateral overgrowth

*Q. Li et al., Appl. Phys. Letts. 106 (7), 072105, 2015*
InAs QD on (001) Si

- GaAs thin films grown on exact (001) Si substrate by MOCVD
  - No Ge, No offcut
- 5x quantum dot microdisk active region was regrown by MBE
  - QD Diameter of $\sim 21$ nm and height of $\sim 6$ nm

<table>
<thead>
<tr>
<th>MBE @UCSB</th>
<th>MOCVD</th>
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<tbody>
<tr>
<td>10 nm GaAs</td>
<td>1 $\mu$m GaAs buffer</td>
</tr>
<tr>
<td>50 nm Al$<em>{0.4}$Ga$</em>{0.6}$As</td>
<td>1 $\mu$m GaAs template</td>
</tr>
<tr>
<td>5-layer InAs/InGaAs DWELL</td>
<td>Exact (001) silicon</td>
</tr>
<tr>
<td>50 nm Al$<em>{0.4}$Ga$</em>{0.6}$As</td>
<td>600 nm Al$<em>{0.7}$Ga$</em>{0.3}$As</td>
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<td>600 nm Al$<em>{0.7}$Ga$</em>{0.3}$As</td>
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<tr>
<td>1 $\mu$m GaAs buffer</td>
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MBE Growth of Quantum Dots @ UCSB

- 5x InAs quantum dot layers
  - 500°C, 0.11 ML/s, 2.75 ML, V/III 35
  - 8 nm In\textsubscript{0.15}Ga\textsubscript{0.85}As QW
- Dot density $\sim5\times10^{10}$ cm\textsuperscript{-2} per layer
- Uniform wavelength across sample
TEM comparison: QD on GoVS and Offcut Si

- A three-fold reduction of threading dislocation using V-grooved Si
- V-grooved Si: 2.8x10^8/cm^2  
  Offcut Si: 8.3 x 10^8/cm^2

*TDD was determined by counting numbers of dislocations in a given area based on an average number of 30 plane-view TEM images for accuracy.
• 1.3 μm room temperature emission
• strong peak intensity
• FWHM of 29 meV

Photoluminescence comparison at 300K
Micro-fabricated WGM cavities

Silica beads deposition

Inductively coupled plasma etching

Silica beads removal

HF selective etching
1.3 μm RT lasing on (001) silicon

- RT CW lasing from a 4 μm disk
- Q~5000, Xc~1.3 μm

1.3 μm RT lasing on (001) silicon

- CW lasing from 4 μm diameter microdisks up to RT
- At RT, single mode lasing at 1.3 μm
Temperature characteristics of 4 μm MDL on (001) silicon

300K laser Spectra below (8 μW) and above (495μW) threshold

10K laser Spectra below (8 μW) and above (495μW) threshold
Comparison of 10K characteristics for different substrates

Q Li, et al., Optics Express 24 (18), p. 21038, 2016
Comparison of 300K characteristics for different substrates

Q Li, et al., Optics Express 24 (18), p. 21038, 2016
Subwavelength microlasers on Si

Pros
- Dense integration
- Low power consumption
- Single mode (well-separated cavity modes)

Cons
- High surface recombination
- Limited gain medium

Free Spectral Range

$$\Delta \lambda \approx \frac{\lambda^2}{2 \pi R_{\text{eff}}} = \frac{[1.2 \mu]^2}{2 \pi (0.5 \mu) 3.46} = 132 \text{nm}$$

Lasing characteristics at 10K

Graphs showing intensity vs. wavelength for different pump powers (165 µW, 82.5 µW, 49.5 µW, 16.5 µW, 8.25 µW) at 10K. The graphs indicate lasing emission at specific wavelengths with peak intensities.

Plot (b) shows the dependence of intensity on wavelength at a pump of 16.5 µW, with a significant peak at 1200 nm labeled as cavity emission.

Plot (d) illustrates the intensity as a function of injection power (uW) with a threshold at 35 µW indicated.

Plot (e) demonstrates the change in FWHM (full width at half maximum) with injection power, showing a decrease with increasing power and a peak at 15dB.
Lasing characteristics at 10K

- Lasing mode: $\text{TE}_{1,5}$ by FDTD simulation

- The spontaneous emission factor ($\beta$) was extracted to be 0.3 by fitting the experimental data to a semiconductor cavity-QED model.

Benchmarking with subwavelength MDL on GaAs

Table. Lasing statistics summary

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<tr>
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<th>Average lasing threshold, μW</th>
<th>Threshold range, μW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>50</td>
<td>35-67</td>
</tr>
<tr>
<td>GaAs</td>
<td>33</td>
<td>24-50</td>
</tr>
</tbody>
</table>

![Graph showing wavelength vs. threshold power for Si and GaAs materials.](image)
Typical GoVS 100mm compliant substrate

3 cycles of thermal cycle annealing

~2.2 μm GaAs

300 nm GaAs

1100 nm GaAs

15 × {5nm GaAs/5nm Al_{0.3}Ga_{0.7}As}

600 nm UID-GaAs

p- (001) Si with nano-pattern

XRD rocking curve
FWHM = 112 arcsec
TDD = 4 × 10^7 /cm^2
(Ayers ‘ Model)
Planar InP nanowires on (001) Si

Challenges

- 8% lattice mismatch leads to high density of defects
- Polarity difference and generation of APBs

Methods to integrate InP NW on Si

- Thick GaAs buffer

LT-InP at 370 °C, V/III ratio >2000

500-nm-wide CMP bulk InP


Growing InP NWs on Si

- 800 nm pitch, 300 nm openings with 150 nm SiO$_2$
- Diamond pocket formed by KOH wet etching
- LT-GaAs buffer and three-step InP growth procedure
LT-GaAs nucleation

- Large indium diffusion coefficient and low TBP decomposition rate
- Complete coverage of LT-GaAs on initial Si enclosure
- LT-GaAs aligned along Si surface and formation of stacking faults

Morphology evolution

Coalescence of InP islands

Rhombic nanowire formation

(111) plane InP contacts with SiO₂
Both Si and InP peaks can be clearly identified.

“Defect necking effect” leads to more defective region at the bottom.

<table>
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<th>XRD ($\omega$-rocking curve)</th>
<th>FWHM (arcsec)</th>
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<td>659</td>
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Defect trapping

- Defects confined within the diamond pocket
- Stacking faults formed along (111) surface to release strain
- Dislocations traveling upwards observed
InGaAs quantum well (QW-1)

- 10 nm flat InGaAs quantum well flush with the diamond pocket
- Uniform thickness across the opening
- Dislocations penetrate QW and terminate at (111) InP surface
Crescent quasi-quantum wire formation at higher position

(111) facet size increases and (001) facet size decreases

Growth rate difference between (001) and (111)
Further elevating position leads to the reduction of lateral size
Quantum confinement from both vertical and lateral direction
No (111) plane InGaAs observed
Room temperature PL measurement

- Broad PL spectrum due to thickness and composition inhomogeneity
- PL enhancement from QW to QWR samples, due to less defect intrusion
“Uncertainty principle” and Detective work

• Consistency of growth system
• Correlation/optimization of a few $M \times N$ matrices ($m$, $n$ variable parameters)

Device layer design parameters => Device characteristics (models and simulation)
Intended device structure => grown device structure
Growth parameters => Material characteristics
Material Characteristics => Device characteristics
Fabrication process => Device characteristics
Where we are in Hong Kong
Acknowledgements